UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,942	05/10/2001	Geofrey S. Strongin	TT3757	5373

23720 7590 03/16/2005

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
LANIER, BENJAMIN E	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,942	STRONGIN ET AL.	
	Examiner	Art Unit	
	Benjamin E Lanier	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 04 January 2005, with respect to the rejection(s)of claim(s) claims 1-29 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chang, U.S. Patent No. 6,286,097.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 11 recites the limitation "the second I/O bus" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 10-16, 18-20, 23-26, 28, 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang, U.S. Patent No. 6,286,097. Referring to claim 1, 12, Chang discloses a computer system for accessing read only memory (ROM) wherein the computer system comprises a main processor (Fig. 8, 310), a bridge coupled to the processor (Fig. 8, 322), a memory selectably coupled to the bridge and the processor (Fig. 8, 350), a switching mechanism coupled between the memory of each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory (Fig. 8, 325 & Abstract).

Referring to claims 2-4, Chang discloses that the booting control circuit (Fig. 8, 323) sends out a signal when the system is booting up, which allows the processor access to the ROM so that the necessary boot information can be shadowed into main memory. After the transfer, the boot control circuit signals to the switching mechanism that the boot process has completed and ROM access is passed to the peripherals (Col. 3, lines 13-27), which meets the limitations of control logic coupled to the switching mechanism for controlling changes between the first state and the second state, a second bridge coupled between the bridge and the processor, wherein the control logic is comprised within or controlled by the second bridge, wherein the control logic is comprised within or controlled by the processor (Fig. 8, 300).

Referring to claim 10, Chang discloses that the memory and the bridge are coupled to an I/O bus (Fig. 8, 350, 322B, 324), wherein the bridge further comprises I/O bus interface logic for communicating to the I/O bus (Fig. 8, 324, 322B), wherein the processor further comprises I/O bus interface logic for communicating to the I/O bus (Fig. 8, 310), wherein the switching mechanism is coupled to the I/O bus (Fig. 8, 325B, 325C), wherein the processor is coupled to

the switching mechanism through the I/O bus interface logic (Fig. 8, 310, 322B, 324, 325B, 325C), wherein the first state comprises the I/O bus interface logic of the processor being configured to communicate with the memory over the I/O bus (Col. 3, lines 13-27, Fig. 8 300), and wherein the second state comprises the I/O bus interface logic of the bridge being configured to communicate with the memory over the I/O bus (Col. 3, lines 18-27, Fig. 8 300).

Referring to claim 11, Chang discloses that the second I/O bus comprises an LPC bus (Fig. 8, 324).

Referring to claim 13, Chang discloses that the ROM is a BIOS ROM (Col. 1, line 53).

Referring to claims 14, 18-20, 23, 24, 28, 29, Chang discloses a computer system comprising a processor (Fig. 8, 310), a memory (Fig. 8, 350), and a first device (Fig. 8, 322), wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory (Fig. 8, 310, 322, 325, 350 & Abstract). Coupling the processor and the memory using a switching mechanism (Fig. 8, 325), wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory (Col. 3, lines 13-27), switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism (Col. 3, lines 13-18), reading from memory in the second state (Col. 4, line 65 – Col. 5, line 2), means for controlling the means for switching (Fig. 8, 323).

Referring to claims 15, 25, Chang discloses the processor is coupled to the first device through at least a system bus (Fig. 8, 310, 322), wherein the first device is coupled to the memory through a first I/O bus (Fig. 8, 322B, 324, 325B, 325C, 350), wherein coupling the

processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism (Fig. 8, 325 A-C).

Referring to claims 16, 26, Chang discloses that the ROM contains BIOS information and that when the computer system boots up the processor accesses the programs stored on the ROM to boot the computer system (Col. 4, line 63 – Col. 5, line 5), which meets the limitation of the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 5-9, 17, 21, 22, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent No. 6,286,097, in view of Davis, U.S. Patent No. 5,844,986. Referring to claim 5-9, 17, 21, 22, 27, Chang discloses a computer system for accessing a BIOS ROM (Col. 1, line 53) wherein the computer system comprises a main processor (Fig. 8, 310), a bridge

coupled to the processor (Fig. 8, 322), a memory selectably coupled to the bridge and the processor (Fig. 8, 350), a switching mechanism coupled between the memory of each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory (Fig. 8, 325 & Abstract). A second bridge coupled between the bridge and the processor (Fig. 8, 310, 322, 323), wherein the second bridge is coupled to the processor through the local bus (Fig. 8, 310, 323), wherein the second bridge is coupled to the bridge through the first I/O bus (Fig. 8, 323, 322B, 324, 325A-C). Chang does not disclose that the ROM is a secure ROM accessible through a crypto-processor. Davis discloses a secure BIOS ROM that is housed within a crypto-processor so that when the computer system boots, the main processor issues a read request for an address corresponding to the BIOS program. The cryptographic processor responds to that request with the associated BIOS instruction (Col. 3, lines 30-34). The main processor processes the data and BIOS instructions (Col. 3, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the secure BIOS ROM of Davis in the ROM accessing system of Chang in order to protect the BIOS ROM for potential viruses and corruption as taught in Davis (Col. 1, lines 62-67).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Evoy, U.S. Patent No. 5,603,055

Rockford, U.S. Patent No. 5,892,943

Le, U.S. Patent No. 5,819,087

Le, U.S. Patent No. 5,794,054

Leung, U.S. Patent No. 6,446,139

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin E Lanier whose telephone number is 571-272-3805. The examiner can normally be reached on M-Th0 7:30am-5:00pm, F 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin E. Lanier

GILBERTO BARRÓN JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100